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0.25 μm Merged Bulk DRAM and SOI Logic using Patterned SOI

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Abstract

The successful fabrication of commodity 64 Mb DRAM chips and logic device and circuits on patterned SOI wafers is reported for the first time. The effect of SIMOX implantation and annealing on DRAMs in patterned SOI wafers is studied. Excellent yields and comparable performance of DRAM in bulk regions of the patterned SOI wafers are observed. The logic devices in the adjacent SOI area of the patterned wafer show the expected enhanced drive current. This approach enables SOI based embedded DRAM.

Introduction

Significant performance improvement in IC devices, as the devices continue to be scaled aggressively below the 0.1μm technology, remains an important driving factor in the IC industry. The use of silicon-on-insulator (SOI) and new materials such as low *k* dielectrics and copper for interconnects is helping to successfully address these challenges [1]. The functional integration of logic and memory devices in the System on a Chip (SoC) is the next logical step for the performance improvement for the subsequent generations [1,2]. Successful SoC on SOI wafers, however, has challenges. Besides possible processing related hurdles for DRAM cells on SOI, the higher leakage introduced by material quality and the history effect resulting from the floating body can have detrimental effect on the performance of DRAM devices on SOI [3]. A possible solution would be to implement SoC on a chip with patterned SOI regions. The high performance logic devices could be fabricated on the SOI portions of the chip and the low leakage DRAM cells on the 'bulk' silicon regions. This paper reports a study of the use of patterned SOI for logic and DRAM integration on adjacent regions of the same wafer. The effects of the implantation and annealing during SOI formation on the DRAM characteristics are also studied.

Experiment

Patterned SOI wafers were fabricated by masking out the oxygen implantation from the bulk regions during the separation by implantation of oxygen (SIMOX) process (Fig.1). Thick buried oxide (BOX) and thin BOX SOI wafers were fabricated to study the effect of the oxygen dose on the DRAM devices located in the adjacent bulk regions. Bulk silicon wafers were annealed along with the thick and thin patterned SOI wafers during the subsequent SIMOX process annealing to study the effect of high temperature SIMOX annealing on the DRAM performance.

Trench capacitor DRAM and logic devices were fabricated on wafers in the experimental wafer-splits shown in Table I. The DRAM fabricated was fully qualified commercial 0.25 μm generation 64 Mb EDO product (16MX4) of IBM Corporation which used 3.3±0.3V external power supply supplemented by an internally generated 2.5V supply. The performance specification for this product is shown in Table II [4].

Results and Discussions

Cross-section transmission electron microscope (XTEM) micrographs of thick and thin patterned SOI wafers are shown in Fig. 2a and 2b. It is observed that the damage at the SOI-region interface is lower for thin BOX than for thick BOX. This is due to the higher oxygen dose used for the thick BOX. Fig. 3 shows cross-section and plan view of the SOI-bulk interface after the fabrication of the DRAM cells. No visible defects are observed in the DRAM active areas adjacent to the SOI-bulk interface made possible through the use of dislocation filtering techniques.

Fig. 4 shows that the median retention time obtained from the 1Mb array diagnostic monitor (ADM) which is seen to be comparable for devices on all wafers. The screen fixable ADM chips yield for the different splits is shown in Fig. 5. Fig. 6 shows the relative fixable yield for 640ms retention of the 64Mb chip. The yield loss in the DRAM in patterned SOI appears to be affected mainly by the implantation rather than the annealing during the SIMOX process. The specifications in Table II were met or exceeded in all cases for good dies.

Fig. 7 shows representative transistor curves for NFET transistors on thick SOI and Bulk on adjacent dies on the patterned wafer. The devices were fabricated using 0.25 μm technology. The I_D-V_D curves for NFET transistors with W=20 μm and L=0.7 μm are shown for different gate bias voltages. A 34% increase in the on-current is observed for the SOI device, although the device is not optimised for SOI substrates. The kink effect that is distinctive for partially depleted devices is also evident from the figure.

Conclusion

We have demonstrated the successful fabrication of high density DRAM on the bulk area of patterned SOI wafers with high performance SOI logic. This process allows for combining of an unmodified DRAM design with high performance SOI based logic, enabling SOI based embedded DRAM.

Acknowledgements

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References

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[3] J. Mandelman, et al., IEEE Int. SOI. Conf., pp.136-137 (1996)
[4] http://www.chips.ibm.com/products/memory/88H2007/

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Wafer Splits	SIMOX implant	SIMOX anneal
Bulk control wafers	No implant	No anneal
Patterned thin BOX	Low dose	Thin SIMOX anneal
Bulk w/low dose anneal	No implant	Thin SIMOX anneal
Patterned thick BOX	High dose	Thick SIMOX anneal
Bulk w/high dose anneal	No implant	Thick SIMOX anneal

Table I. The wafer-splits to study the effect of patterned SOI on DRAM device performance.

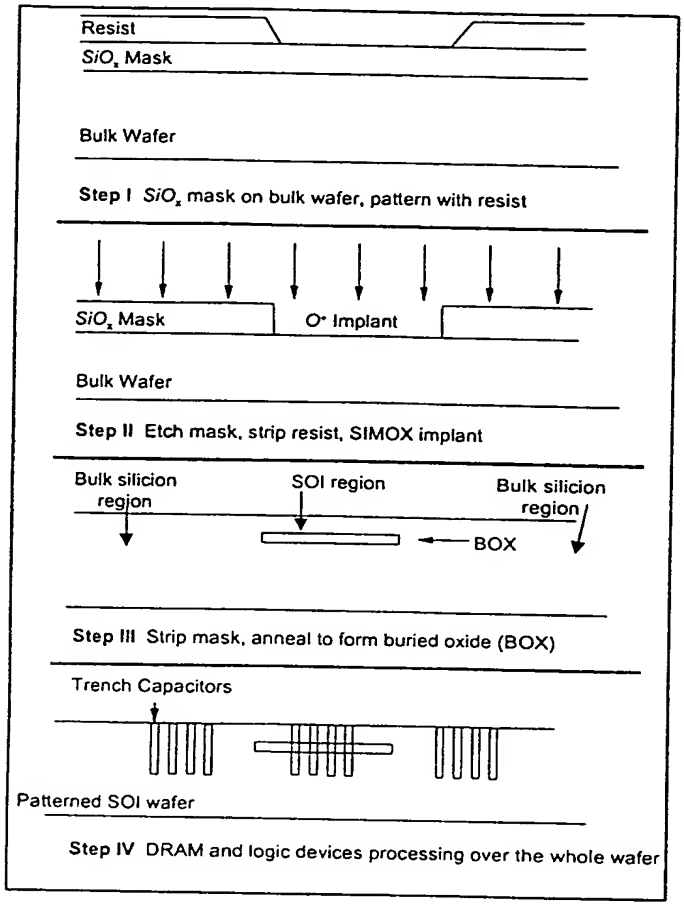

Fig. 1 Schematic of the patterning process used for the experiment.

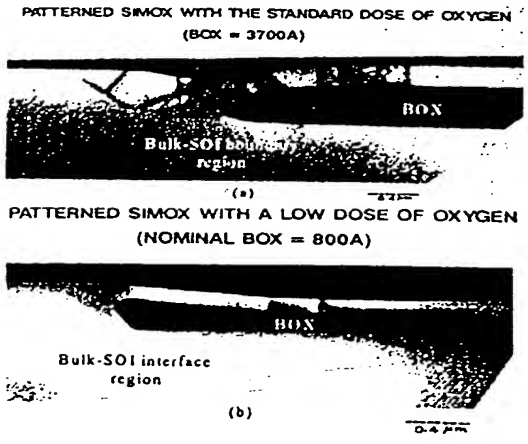

Fig. 2 (a) Bulk-SOI boundary for thick BOX and (b) Bulk-SOI boundary for thin BOX. Damage is more for thick BOX compared to thin BOX.

		-50	-60
t_{RAC}	RAS Access Time	50ns	60ns
t_{CAC}	CAS Access Time	13ns	15ns
t_{AA}	Column Address Access Time	25ns	30ns
t_{RC}	Cycle Time	84ns	104ns
t_{HPC}	Hyper Page Mode Cycle Time	20ns	25ns

Table II. The performance specification of the 64 Mb DRAM fabricated [4].

Fig. 3 Top view (left) and Cross-section view (right) of the bulk-SOI interface region.

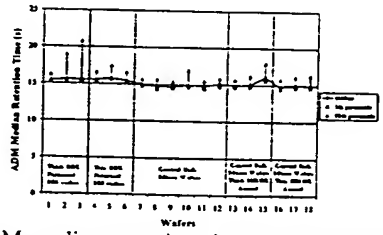

Fig. 4 The ADM median retention time are comparable for all the splits.

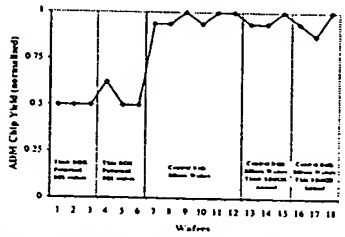

Fig. 5 Relative screen fixable chip yield for the ADM

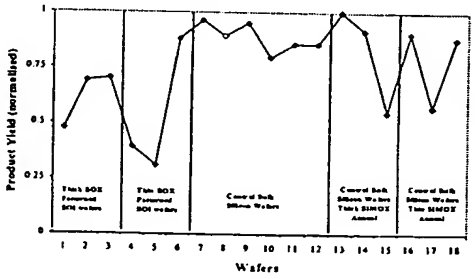

Fig. 6 Relative fixable yield for a 640 ms retention of 64 Mb chip.

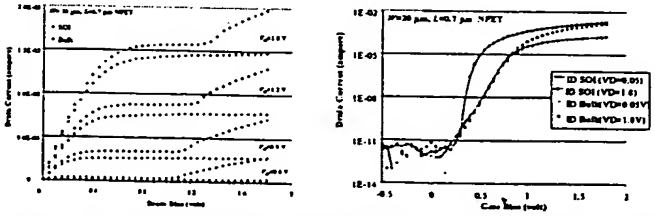

Fig. 7 The logic devices in adjascent SOI and bulk regions of the patterned SOI. Devices on SOI exhibit the kink effect and an increased drive current.